Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The final Office Action dated October 17, 2005, indicated that claims 1-19 are rejected under 35 U.S.C. § 102(b) over *Daniels et al.* (U.S. Patent No. 4,203,157); claims 1-19 are rejected under 35 U.S.C. § 112(2); and claim 20 is allowable.

Applicant appreciates the allowability of claim 20.

Applicant respectfully traverses each of the Section 112(2) rejections because the claims distinctly point out the subject matter of the present invention. It would appear that the Examiner has misinterpreted the meaning of the claims by asserting a nonexistent requirement of Section 112. The Examiner's assertion regarding the alleged inoperability of a single claimed combination, even if correct, is not a proper basis for a Section 112 rejection. *See, e.g., In re Dinh-Nguyen*, 492 F.2d 856, 858-59, 181 USPQ 46, 48 (CCPA 1974) (stating that a claim is not necessarily invalid even if some of the claimed combinations are inoperative).

Accordingly, Applicant submits that the premise underlying the §112 rejection is not supported by the law. Moreover, with respect to the rejections of independent claims (claims 1, 18 and 19) where the Examiner asserts that the claims are mis-descriptive, Applicant respectfully traverses. Under the above-discussed law, claims 1-19 are indefinite as they set forth an invention embracing at least a number of enabled embodiments.

Turning now to this technical single-embodiment argument raised in the Office Action, the Examiner argues that (i) N needs to be greater than M if the multiplexer outputs a most significant bits (MSBs) partial sum, and (ii) that the selection data is a function of the MSB of the set of LSBs of the second, not first, binary operand. In summary, it would appear that the issue is whether N can be equal to M.

First, Applicant submits that N need not necessarily be greater than M because the claimed invention permits this configuration, N equal to M. Thus, by definition, the scope of claimed invention permits for this situation.

Second, Examiner is wrong in arguing that N must be greater than M if the multiplexer outputs an MSB partial sum. Examiner's assertion (that where "N – M = 0 there is [no] partial sum") assumes that where N equals M, a representative set of MSB

cannot exist. This argument carries the unsupported/flawed rationale (as addressed previously) that assumes partial sums cannot be performed on numbers of equal bits. By repeating this argument (note the requirements of MPEP 707.07(f)), the Examiner fails to adequately consider and respond to Applicant's prior assertion that the multiplexer can output an MSB partial sum whether N is greater than M, or N is equal to M. This situation can arise, for example, because the multiplexer can output an MSB partial sum whenever the multiplexer passes "a representative set of most-significant bits of the first binary operand", as set forth in claim 1. Put another way, the multiplexer output of an MSB partial sum is not precluded when N equals M because it can still be supplied a representative set of most-significant bits. Consider, for example, a situation where N and M are both equal to eight; an MSB partial sum of the bits four to seven could be taken. Moreover, the MSB and LSB sets are not claimed to be mutually exclusive, allowing for LSB and MSB sets to potentially contain some of the same bits. Accordingly, the first-mentioned rationale "(i)" is flawed.

Examiner erroneously argues that (ii) the selection data is a function of the MSB of the set of LSBs of the second, not the first, binary operand. This aspect of the invention is supported, for instance, in the Specification at page 6, lines 5-13 (particularly the clause at page 6 lines 22-23). Examiner asserts that Equation B, illustrated by Fig. 3 and implemented in Fig. 4, shows that the first operand is not used for the selection of the multiplexer output. Examiner's assertion fails to note that Fig. 3 and Fig. 4 also show selection bit C15. Applicant submits that C15 is a function of the MSB of the set of LSBs of the first binary operand. Moreover, the Specification at page 15, line 5, describes Fig. 4 as "one example" and further describes Fig. 3 as "an example" at page 5, line 1. Accordingly, the second-mentioned rationale "(ii)" is flawed.

With respect to claims 16 and 17, the Examiner asserts that the claimed digital filtering circuit arrangement is inconsistent with claim 1 because claim 1 is "limited to an adder circuit." Applicant fails to understand the Examiner's rationale but notes that claim 1 is directed to a circuit arrangement that includes an adder and a multiplexer circuit and is in no way limited to an adder circuit. The arrangement of claim 1 is available for implementation as a digital filtering arrangement and Applicant accordingly requests that the rejection be withdrawn.

Applicant also respectfully traverses the Section 102(b) rejection because Examiner fails to present a reference that corresponds to the claimed invention. More specifically, Examiner has cited a reference that appears to be largely unrelated to the claimed invention, and the Examiner fails to identify even the basic claim limitations of the Applicant's invention including, for example, the claimed multiplexer. Nowhere does Examiner attempt to identify where the '157 reference teaches any use of a multiplexer.

While the Examiner refers to the Abstract, the Abstract does not mention "multiplexer" or anything that could be taken to resemble multiplexer. In an abundance of caution, Applicant has performed a word search throughout the '157 reference (via the USPTO patent database), and "multiplexer" is not found.

Moreover, the Examiner has not even attempted to explain how any "multiplexer" teaching might be adapted to provide the outputs claimed. Specifically in this regard, Examiner fails to show where Daniels teaches a multiplexer circuit capable of passing, "an output a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand". Moreover, Examiner fails to identify the selection data being a function of the MSB as claimed. Regarding the selection data, Examiner references the last line of the abstract. The Applicant fails to recognize any correspondence between the cited reference and the claimed invention.

Further, Examiner fails to even assert that any of the limitations of the dependent claims are taught by the '157 reference. The following are a few examples of limitations not addressed by the Examiner: "the M-bit adder" of claim 2; "the first binary operand incremented by one....first binary operand decremented by one" in claim 3; "N is 24 and M is 16" in claim 4; "first incremented offset, and a second decremented offset" in claim 5; and "the multiplexer circuit is further configured to operate as an exclusive-or gate: in claim 14.

Without a presentation of correspondence to each of the claimed limitations, the Section 102(b) rejection cannot be maintained. Applicant accordingly requests that the rejection be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Mr. Peter Zawilski, of Philips Corporation at (408) 474-9063.

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